AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended): A data converter for converting an input signal to a digital signal, the data converter comprising:

n comparison units for respectively comparing the input signal with n reference signals to generate the ~~corresponding~~ digital signal, each of the comparison units including a positive output end and a negative output end, the digital signal being generated according to a positive output and a negative output of the comparison units in a differential manner; and

n switch circuits respectively electrically connected to the positive output end and the negative output end of the n comparison units; wherein for a k^{th} comparison unit, ~~the corresponding~~ a k^{th} switch circuit corresponding to the k^{th} comparison unit is further electrically connected to ~~the~~ a positive output end of ~~the~~ a k^{th}-1 comparison unit and ~~the~~ a negative output end of ~~the~~ a k^{th}+1 comparison unit;

wherein when the k^{th} comparison unit performs an auto-zeroing process, the k^{th} switch circuit generates a digital signal corresponding to an interpolated value of the k^{th} comparison unit from ~~a~~ the positive output of the k^{th}-1 comparison unit and ~~a~~ the negative output of the k^{th}+1 comparison unit.

Claim 2 (original): The data converter of claim 1 wherein each of the comparison units comprises a latching circuit for outputting the digital signal.

Claim 3 (currently amended): The data converter of claim 1 wherein each of the comparison units comprises an amplifier for amplifying a voltage difference between the input signal and ~~the corresponding~~ a reference signal so as to generate a corresponding positive output and a corresponding negative output.

Claim 4 (original): The data converter of claim 3 wherein each of the comparison

units further comprises a feedback circuit electrically connected between an output end and an input end of the amplifier, and when the comparison unit performs the auto-zeroing process, the feedback circuit conducts.

Claim 5 (original): The data converter of claim 1 wherein the data converter further comprises a voltage dividing circuit for generating the n reference signals.

Claim 6 (currently amended): A method for a data conversion circuit for converting an input signal to a ~~corresponding~~ digital signal, the data conversion circuit comprising:

n comparison units for respectively comparing the input signal with n reference signals to generate the ~~corresponding~~ digital signal, each of the comparison units including a positive output end and a negative output end, the digital signal being generated according to a positive output and a negative output of the comparison units in a differential manner, the method comprising:

when a k^{th} comparison unit is performing an auto zeroing process, substituting the digital signal of the k^{th} comparison unit with a replacement signal generated according to outputs of ~~the~~ a positive output end of ~~the~~ a k^{th}-1 comparison unit and ~~the~~ a negative output end of ~~the~~ a k^{th}+1 comparison unit, such that when the output of the positive output end of the k^{th}-1 comparison unit is less than the output of the negative output end of the k^{th}+1 comparison unit, the replacement signal is a first digital value, and when the output of the positive output end of the k^{th}-1 comparison unit is greater than the output of the negative output end of the k^{th}+1 comparison unit, the replacement signal is a second digital value.

Claim 7 (original): The method of claim 6 wherein the first digital value is a high logical value, and the second digital value is a low digital value.

Claim 8 (currently amended): A data converter for converting an ~~analog~~ input signal to

a plurality of digital bits, the data converter comprising:

n first comparison units for respectively comparing the input signal with n reference signals, each of the comparison units including a positive output end for outputting a first positive output and a negative output end for outputting a first negative output;

n second comparison units for respectively comparing the input signal with the n reference signals, each of the second comparison units including a positive output end for outputting a second positive output and a negative output end for outputting a second negative output; and

an output unit electrically connected to the n first comparison units and the n second comparison units for generating digital bits corresponding to the n first comparison units and the n second comparison units, the output unit comprising:

n-1 interpolating units electrically connected to the n first comparison units and the n second comparison units, a k^{th} interpolating unit being electrically connected to a k^{th} and a ~~k^{th+1}~~ $k^{th}+1$ first comparison units and a k^{th} and a $k^{th}+1$ second comparison ~~unitsfor~~ units for adding a third positive output to the first and second positive outputs of the ~~nfirst~~ n first comparison units and the ~~nsecond~~ n second comparison units and adding a third negative output to the first and second negative outputs of the ~~nfirst~~ n first comparison units and the ~~nsecond~~ n second comparison units; wherein when the k^{th} and the $k^{th}+1$ first comparison ~~unitsperform~~ units perform an auto-zeroing process, the k^{th} interpolating unit is capable of utilizing the second positive outputs of the k^{th} and the $k^{th}+1$ second comparison units for generating the third positive output and utilizing the second negative outputs of the k^{th} and the $k^{th}+1$ second comparison units for generating the third negative output;

wherein the output unit generates a digital bit interpolated between a digital bit corresponding to the k^{th} second comparison unit and a digital bit corresponding to the $k^{th}+1$ second comparison unit according to the third

positive output and the third negative output in a differential manner.

Claim 9 (currently amended): The data converter of claim 8 wherein the output unit further comprises a plurality of latches electrically connected to the first comparison units, the second comparison units, and the interpolating units for outputting the digital bits.

Claim 10 (currently amended): The data converter of claim 8 wherein each of the first and second comparison units comprises an amplifier for amplifying a voltage difference between the input signal and ~~the corresponding~~ a reference signal so as to generate a corresponding positive output and a corresponding negative output.

Claim 11 (original):The data converter of claim 10 wherein each of the first and second comparison units further comprises a feedback circuit electrically connected between an output end and an input end of the amplifier, and when the comparison unit performs the auto-zeroing process, the feedback circuit conducts.

Claim 12 (original):The data converter of claim 8 wherein the data converter further comprises a voltage dividing circuit for generating the n reference signals.

Claim 13 (original): The data converter of claim 8 wherein the third positive output is interpolated between the second positive output of the k^{th} and the $k^{th}+1$ second comparison units, and the third negative output is interpolated between the second negative output of the k^{th} and the $k^{th}+1$ second comparison units.

Claim 14 (currently amended): A method for a data converter for converting an ~~analog~~ input signal to a plurality of digital bits, the data converter comprising:

n first comparison units for respectively comparing the input signal with n reference signals, each of the comparison units including a positive

output end for outputting a first positive output and a negative output end for outputting a first negative output, a digital bit corresponding to a first comparison unit being generated from the first positive output and the first negative output in a differential manner;

n second comparison units for respectively comparing the input signal with the n reference signals, each of the second comparison units including a positive output end for outputting a second positive output and a negative output end for outputting a second negative output, a digital bit corresponding to a second comparison unit being generated from the second positive output and the second negative output in a differential manner, the method comprising:

when a k^{th} and a $k^{th}+1$ first comparison units perform an auto-zeroing process, utilizing the second positive outputs of a k^{th} and a $k^{th}+1$ second comparison units for generating a third positive output, utilizing the second negative outputs of the k^{th} and the $k^{th}+1$ second comparison units for generating a third negative output, and generating a digital bit interpolated between a digital bit corresponding to the k^{th} second comparison unit and a digital bit corresponding to the $k^{th}+1$ second comparison unit according to the third positive output and the third negative output in ~~the~~ a differential manner.

Claim 15 (currently amended): The method of claim 14 wherein the third positive output is interpolated between ~~thesecond~~ the second positive outputs of the k^{th} and the $k^{th}+1$ second comparison units, and the third negative output is interpolated between the second negative outputs of the k^{th} and the $k^{th}+1$ second comparison units.

Claim 16 (currently amended): A data converter for converting an ~~analog~~ input signal to a plurality of digital bits, the data converter comprising:

n first comparison units for respectively comparing the input signal with n reference signals, each of the comparison units including a positive output end for outputting a first positive output and a negative output

end for outputting a first negative output;

n second comparison units for respectively comparing the input signal with the n reference signals, each of the second comparison units including a positive output end for outputting a second positive output and a negative output end for outputting a second negative output; and

an output unit electrically connected to the n_first comparison units and the n second comparison units for generating digital bits corresponding to the n_first comparison units and the n second comparison units, the output unit comprising:

n-1 interpolating units electrically connected to the n first comparison units and the n second comparison units, a k^{th} interpolating unit being electrically connected to a plurality of (k^{th} to ~~k^{th+p}~~$\underline{k^{th}+p}$) first comparison units and a plurality of (k^{th} to ~~k^{th+p}~~$\underline{k^{th}+p}$) second comparison units for adding a plurality of positive outputs to the first and second positive outputs of the ~~nfirst~~ n first comparison units and the ~~nsecond~~ n second comparison units and adding a plurality of negative outputs to the first and second negative outputs of the ~~nfirst~~ n first comparison units and the ~~nsecond~~ n first comparison units; wherein p is an integer, and when some first comparison units perform an auto-zeroing process, the k^{th} interpolating unit is capable of utilizing the second positive outputs of the ~~plurality of~~ second comparison units for generating a plurality of positive outputs and utilizing the second negative outputs of some second comparison units for generating some negative outputs;

wherein the output unit generates a digital bit interpolated between a digital bit corresponding to the k^{th} second comparison unit and a digital bit corresponding to the ~~k^{th+p}~~$\underline{k^{th}+p}$ second comparison unit according to the positive outputs and the negative outputs in a differential manner.

Claim 17 (currently amended): The data converter of claim 16 wherein the output unit further comprises a plurality of latches electrically connected to the first

comparison units, the second comparison units, and the interpolating units for outputting the digital bits.

Claim 18 (currently amended): The data converter of claim 16 wherein each of the first and second comparison units comprises an amplifier for amplifying a voltage difference between the input signal and ~~the corresponding~~ a reference signal so as to generate a corresponding positive output and a corresponding negative output.

Claim 19 (original): The data converter of claim 18 wherein each of the first and second comparison units further comprises a feedback circuit electrically connected between an output end and an input end of the amplifier, and when the comparison unit performs the auto-zeroing process, the feedback circuit conducts.

Claim 20 (currently amended): The data converter of claim 16 wherein each of the positive outputs is interpolated between the second positive outputs of the k^{th} ~~to~~ and the ~~k~~$^{th+p}$ $k^{th}+p$ second comparison units, and ~~the~~ each of the negative output is interpolated between the second negative outputs of the k^{th} and the ~~k~~$^{th+p}$ $k^{th}+p$ second comparison units.